

associated with one of two addresses, one which directs interpolation of the pixel as a video pixel through video front-end pipeline 200 and the other which directs interpolation of the pixel as a graphics pixel through write buffer 207 and graphics controller 208. As a consequence, either video or graphics pixel data can then be input to CPU interface 206 from the PCI/VI bus through a single "dual aperture" port as a function of the selected address held in an address buffer.--

REMARKS

This Amendment is being filed in response to the Examiner's Final Office Action of January 14, 2002. By this Amendment, the specification has been amended, as agreed upon with the Examiner during a personal interview held on February 20, 2002. Since the amendment raises no question of new matter, as discussed, entry of this Amendment is respectfully requested.

For the reasons given, Applicants believe that the application is in condition for allowance and Applicant requests that the Examiner give the application favorable consideration and permit it to issue as a patent.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at page 5, line 52, has been amended as follows:

In the preferred embodiment of system 100, CPU 101 can write video data and/or read and write graphics data to frame buffer 107 via CPU interface 206. In particular, CPU 101 can direct each pixel to the frame buffer using one of two maps depending on whether that pixel is a video pixel or a graphics pixel. In the preferred embodiment, each word of pixel data ("pixel") is associated with one of two addresses, one which directs interpolation of the pixel as a video pixel through video front-end pipeline 200 and the other which directs interpolation of the pixel as a graphics pixel through write buffer 207 and graphics controller 208. As a consequence, either video or graphics pixel data can then be input to CPU interface 206 from the PCI/VI bus through a single "dual aperture" port as a function of the selected address held in an address buffer.

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